Docket No.: SON-2010
(80001-2010)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hisao Hayashi et al.

Application No.: 09/772,986 Confirmation No.: 2637

Filed: January 31, 2001 Art Unit: 2811

For: THIN FILM SEMICONDUCTOR DEVICE, DISPLAY DEVICE USING SUCH THIN FILM SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Examiner: T. F. Tran

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on October 6, 2004.

All arguments presented within the Appeal Brief of July 7, 2004 are incorporated herein by reference. Additional arguments are provided hereinbelow.

Claim 14 includes the features of:

an insulating substrate; and

a thin film transistor formed on said insulating substrate, wherein:

said thin film transistor is formed in a bottom gate structure having gate electrode, a gate insulating film, and a semiconductor thin film stacked in the order from below upward,

said gate electrode is made of metallic material having a thickness of less than 100nm,

said gate insulating film has a thickness that is greater than said thickness of said gate electrode,

the thickness of the gate insulating film is greater than 100 nm, and

the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.

Claim 16 includes the features of:

an insulating substrate;

pixels arranged in a matrix form;

thin film transistors for driving said respective pixels, wherein said pixels and said thin film transistors are formed as integrated circuits on said insulating substrate, each of said thin film transistors has a bottom gate structure having a gate electrode, a gate insulating film and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100 nm,

said gate insulating film has a thickness that is greater than said thickness of said gate electrode,

wherein the thickness of the gate insulating film is greater than 100 nm, and

wherein the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.

Claims 14 and 16 were rejected under 35 U.S.C. §103 as being unpatentable over Japanese Publication No. 10-209467 to Hayashi et al. (Hisao).

Within the claims, the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.

Paragraph [0012] of Hisao arguably teaches a gate electrode 5 having a top layer 5a having a thickness of around 50 to 300 nm and a bottom layer 5b that is set in the range of 50 to 200 nm.

The Examiner's Answer further contends that a gate thickness of 99.99 nm of the gate electrode 5 clearly meets the claim limitation that requires a gate electrode having a thickness of less than 100 nm (Examiner's Answer at page 5). Nevertheless, the Examiner's Answer fails to identify any authority for its conclusion that the combined thickness top layer 5a and bottom layer 5b would necessarily result in gate electrode 5 having a thickness of less than 100 nm. Instead, the Examiner's Answer acknowledges that Hisao fails to specifically disclose the thickness of the gate electrode 5 being 90 nm (Examiner's Answer at page 4).

But as a gap-filler, the Examiner's Answer asserts that *it is obvious as described in appellant's specification that the gate thickness of 99.99 nm and 90 nm would provide the same advantage* (Examiner's Answer at page 7).

In response, the Examiner's Answer fails to show where within the appellant's specification that the asserted description is to be found.

Moreover, this assertion is the essence of hindsight reasoning. Where the prior art must provide a motivation or reason for the skilled artisan to make the necessary changes in Hisao without the benefit of the appellant's specification, the Examiner's Answer impermissibly refers to the appellant's specification to make the necessary changes within Hisao. Thus, this unsupported assertion amounts to nothing more than conclusions that are personal in nature and that are based upon hindsight reasoning.

The Examiner's Answer contends that changes in size and shape of parts in the absence of unexpected results involve only routine skill in the art (Examiner's Answer at page 5).

In response, the Examiner must consider all evidence of nonobviousness when assessing patentability. Specifically, figure 3 of the above-identified application is a graph depicting the relation between a film thickness of gate electrodes and a process margin, whereas figure 4 of the above-identified application is a graph depicting the relation between a film thickness of the gate electrodes and a quantity of pinholes. These figures show that the claimed range achieves unexpected results relative to the prior art range. However, the Examiner's Answer has failed to consider this evidence of nonobviousness when assessing patentability.

Conclusion

The prior art of record, either individually or as a whole, fails to disclose, teach or suggest all the features of the claimed invention. For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained.

Therefore, a reversal of the rejection of March 12, 2004 is respectfully requested.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: December 6, 2004

Respectfully submitted,

By_____

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